An Architecture for TSI-Free Nonblocking Optical TDM Switches

Chin-Tau Lea, *Senior Member, IEEE*, Bey-Chi Lin, and Hamdi Mounir

***Abstract*—One of the key elements in building a time-division-multiplexed (TDM) switch is the time slot interchange (TSI). Given the current optical switching and buffer technologies, TSI-based TDM architectures have many implementation drawbacks, including severe signal attenuation. Some studies showed that some space-time equivalence diagrams can be converted into a delay-unit-based (TSI-free) TDM. This type of architecture is attractive for optical TDM switches, but the techniques discussed in those studies are for rearrangeable switches. Many applications require nonblocking switches where adding a new connection (or a flow) will not cause rearrangement of existing connections. In this paper, we present the design principle for building strictly nonblocking delay-unit-based (TSI-free) optical TDM switches.**

***Index Terms*—Photonic switching system, space/time diagrams, strictly nonblocking (SNB) switches, time slot interchange (TSI).**

I. Introduction

PHOTONIC switching is a relatively new field compared with electronic switching [1]. Photonic switching devices usually exhibit different characteristics than their electronic counterparts. New photonic switching architectures are needed to exploit these differences. For example, some photonic switching devices, such as a directional coupler or a micro-electromechanical systems (MEMS) device, allow two traversing signals, but an electronic switching device only allows one. This characteristic was exploited in [2] to build a more cross-point efficient switch. Another example is a crosstalk reduction, which is a critical issue in an all-optical network, as optical amplifiers are mostly linear amplifiers and cannot remove crosstalk from the system. Although a crosstalk is a device-level problem, it can be solved at the system level with a right switching architecture [3], [4].

This paper deals with another characteristic of photonic switching technologies: the lack of versatile optical buffers. In a conventional time-division-multiplexed (TDM) switch, the time slot interchange (TSI) is a key component that performs time-domain switching. A TSI can be easily implemented with the random access memory. But, its implementation in the optical domain is complicated. One way to build an optical TSI is shown in Fig. 1, and it combines optical space switch and fiber delay lines. A data block will be circulated back into the switch fabric many times before it is sent out [13], [14]. As pointed in [6], signal attenuation can become a severe problem in such a system. The feedback nature also makes synchronization a complicated issue to deal with.

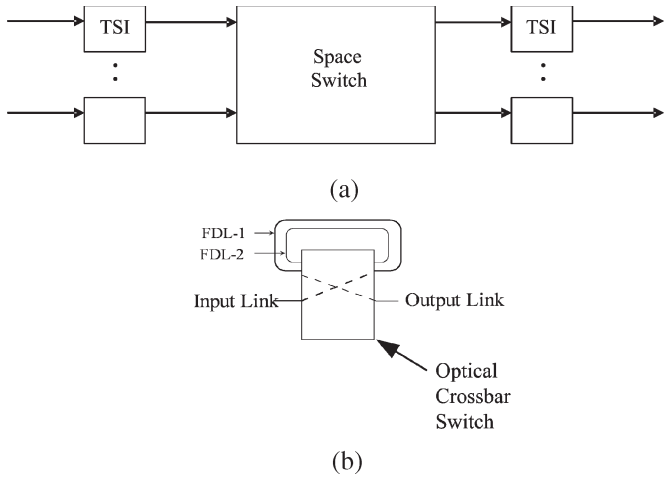

Fig. 1. (a) TSI-based TDM switch. (b) One implementation of an optical TSI.

A TDM switch combines both time and space switching. The design is based on the space/time equivalence principle which has well been discussed. Different space-time equivalence diagrams lead to different types of implementations. One type of diagrams [5], [6] can lead to a TDM switch without using TSIs (see Fig. 2). This TSI-free TDM architecture is very attractive for the reason mentioned above. The techniques discussed in [5] and [6] are for rearrangeable networks where adding a connection (or a flow) may require the rearrangement of existing connections (or flows), but many applications require nonblocking networks [9], [10], in which adding a connection does not affect the existing connections. Nonblocking switches will be the focus of this paper. Hunter and Smith [16] show a delay-unit-based TSI-free strictly nonblocking (SNB) network. It is based on the Cantor network that uses multiple copies of the Benes-like topology discussed in [6]. The TSI-free SNB network design principle discussed in this paper will be more general and more crosspoint efficient than those based on the Cantor network.

There are two types of nonblocking switches: wide-sense nonblocking and SNB. The connection setup in a wide-sense nonblocking network needs to follow a specific algorithm.

Manuscript received April 8, 2006; revised November 4, 2006. This work was supported by the Hong Kong ITF under Grant GHS-025-04.

C.-T. Lea and B.-C. Lin are with the Department of Electronics and Electrical Engineering, Hong Kong University of Science and Technology (HKUST), Hong Kong (e-mail: eelea@ee.ust.hk; eebeychi@ee.ust.hk).

H. Mounir is with the Department of Computer Science, Hong Kong University of Science and Technology (HKUST), Hong Kong (e-mail: hamdi@cs.ust.hk).

Digital Object Identifier 10.1109/JLT.2006.890437

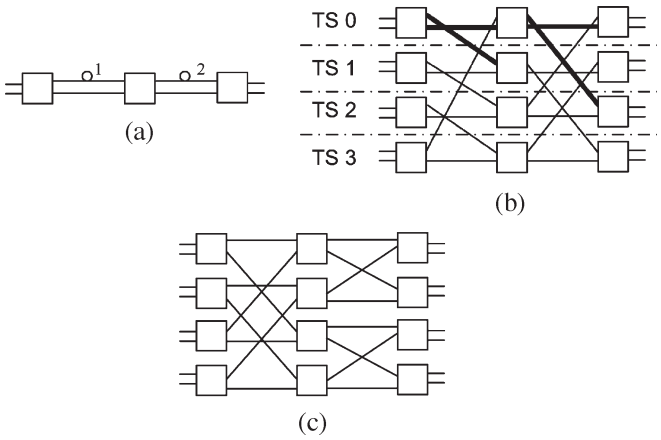

Fig. 2. (a) TDM switch can be implemented with delay units only and does not contain any TSIs. The frame size is four in this example. (b) Time-dilated topology of the TDM switch of (a). We find that once the first n connections are determined, the entire topology is determined. (c) This topology cannot be time compressed into a TDM switch.

But in a SNB network, whenever a path is found, it can be used and no setup algorithms are needed. Generally, wide-sense nonblocking switches require less hardware, but an efficient setup algorithm is also difficult to find. The studies in [11] and [15] showed that for the type of switches discussed in this paper [called $\mathrm{Log}_d(N,k,c)$ networks, see Section II], the two have the same complexity. Thus, we focus on SNB switches in this paper.

A TDM switch is said to maintain frame integrity if data blocks entering one frame will leave the switch in the same frame. Hunter and Smith [6] showed two designs in which one can maintain frame integrity and the other does not. In this paper, we focus on the switches without frame integrity because it is easier to explain our design techniques. Also, the space/time principle can be converted into space/wavelength switching [7], [8], and the frame integrity has no equivalence in the space/wavelength switching. Like the studies in [6] and [8], we also use 2×2 directional couplers to illustrate the design principle. The techniques discussed in this paper can certainly be used for other photonic switching devices of different sizes.

II. Characteristics of a TDTS Topology

A TDM switch involves switching in both the time and space domains. To analyze the switching capability, we usually expand its topology in the time domain so that the entire switching capability can be analyzed in the expanded topology [5], [6]. In a delay-unit-based (TSI-free) **time-dilated TDM switch (TDTS) topology**, also called a space-time diagram in [6], each link is shifted in time by the number of delay units of the link. An example is given in Fig. 2. The TDTS topology contains the entire switching function in both the time and space domains.

A TDTS topology has some important properties that lay the foundation of our design. In the TDTS topology of an $n \times n$ TDM switch with the frame size $= d$, an input can be labeled as (t,s), $0 \le t \le (d-1)$ and $0 \le s \le (n-1)$, where t and s correspond to the time and space dimensions [Fig. 2(b)]. The connection pattern of stage i can be represented as a mapping from the output links of the node stage i to the input links of the node stage $(i+1)$ (Fig. 3). We use $(t,s)_l \mapsto (u,\nu)_r$ to denote the mapping for any stage, where the subscript l and r represent the link positions on the left and right. Because a TDTS topology is a repetition of the connection pattern of the first slot, once the mapping for the first n links $(0,j)_l$, $0 \le j \le (n-1)$ is determined [the heavy lines in Fig. 2(b)], the mapping for the remaining links in that stage is also determined. Fig. 2(b) shows one example where the heavy lines determine the entire TDTS topology of the network.

Property 1: A network topology with size $(nd \times nd)$ is a TDTS topology with input $= n$, frame size $= d$ if and only if

$$(i,j)_l \mapsto (u,\nu)_r \quad \text{then } ((i+e) \bmod d, j)_l \mapsto ((u+e) \bmod d, \nu)_r . \quad (1)$$

This holds for every stage.

Proof: Property 1 is a direct result of a TDTS topology. It is therefore a necessary condition. Conversely, if a network topology satisfies (1), then given the mapping for the first n connections $(0,j)_l$, $0 \le j \le (n-1)$, we can use (1) to generate the mapping for the remaining connections $(r,j)_l$, $1 \le r \le (d-1)$, $0 \le j \le (n-1)$, and they are just a repetition in time of the first n connections. It can be time compressed into a delay-unit-based TDM switch. Thus, Property 1 is also a sufficient condition. ■

In our discussion below, a topology that satisfies (1) is called a **legal** TDTS topology. Property 1 indicates that the degree of freedom in selecting the interconnection patterns for TDTS topologies is much lower than for a general $(nd \times nd)$ switch.

Property 2: Suppose we change the mapping of a given stage of a legal TDTS topology to its inverse mapping, the resulting topology is still a legal TDTS topology.

Proof: Suppose that the given legal TDTS topology has the number of inputs $= n$ and frame size $= d$, and the mapping of the given stage is $(i,j)_l \mapsto (u,\nu)_r$. Its inverse mapping can be written as $(u,\nu)_l \mapsto (i,j)_r$. By Property 1, we have $((i+e) \bmod\ d, j)_l \mapsto ((u+e) \bmod\ d, \nu)_r$. This means that $((u+e) \bmod d, \nu)_l \mapsto ((i+e) \bmod d, j)_r$ is true in the inverse mapping. Thus, the inverse mapping also satisfies Property 1 and the topology of the inverse mapping of a legal TDTS topology is also a legal TDTS topology. ■

Any legal TDTS topology can be time compressed into a delay-unit-based TDM switch. For example, the topology in Fig. 2(b) is a legal space-time diagram, but the topology in Fig. 2(c) is not. Identifying an interconnection topology that satisfies Property 1 is a key step in our design.

III. SNB TSI-Free TDM Switch

A. Design Principle Overview

Shyy and Lea [12] showed a class of nonblocking switches, called $\mathrm{Log}_2(N,k,c)$ networks, created by vertically stacking c copies of an $N \times N$ space switch. The $N \times N$ space switch has a regular structure and $\log_2 N + k$ stages. The extra k stages

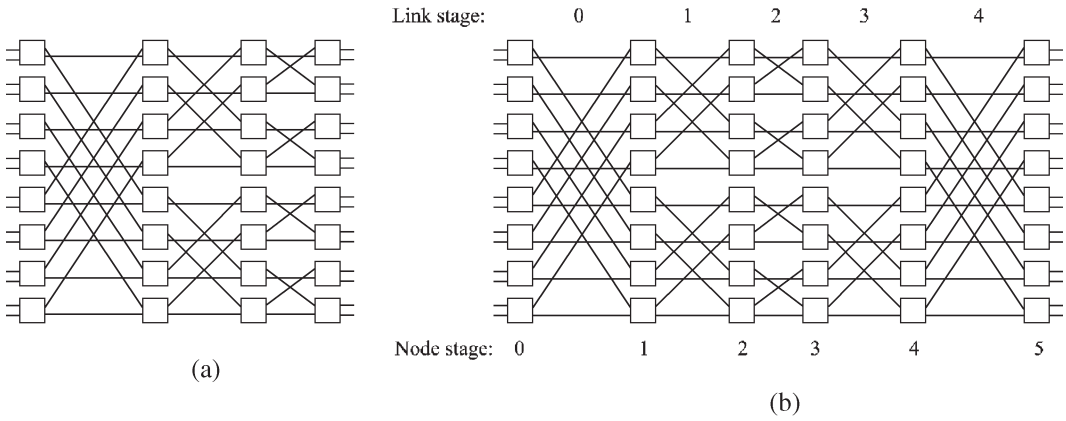

Fig. 3. (a) Banyan networks, BY (4, 0). (b) Banyan with extra stages, BY (4, 2). Note the definition of link stage and node stage in the topology.

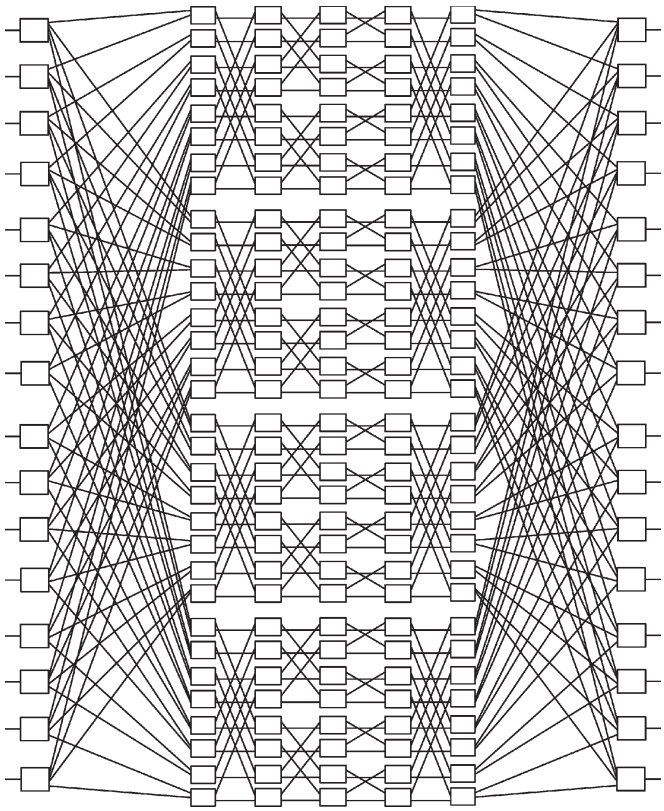

Fig. 4. To construct a TSI-free TDM switch with four inputs and four slots (frame size), the first step is to find a $\mathrm{Log}_2(16, 1, 4)$ network.

are the mirror image of the first k stages in the original $\log_2 N$ stages. There are many types of networks that can be used in the construction of the $\mathrm{Log}_2(N, k, c)$ network. We choose the type given in Fig. 3. The connection pattern is slightly changed from a banyan network (BY) used in [12] (output lines 0 and 1 are swapped). We use $\mathrm{BY}(w, 0)$ to represent a w-stage BY network, and $\mathrm{BY}(w, k)$ to represent a w-stage BY network with k extra stages added. The extra k stages are the mirror image of the first k stages in the BY network. The optimal values of c and k are given in [12]. Fig. 4 shows an example of four copies of BY networks vertically stacked.

The $\mathrm{Log}_2(N, k, c)$ network cannot be directly used to build a TSI-free TDM switch because each copy does not have a legal TDTS topology. But, we can change the topology to one that is a legal TDTS topology with the same switching capability. Let n be the number of input and output TDM switch links and d be the number of timeslots per frame. Assume $n = 2^p$ and $d = 2^q$ (i.e., both are a power of 2). The time-dilated topology of this network will have the size $(nd \times nd)$. The proposed method of constructing a TSI-free TDM switch consists of three steps.

1) Select $N = nd$. Construct the topology of a $\mathrm{Log}_2(N, k, c)$ SNB network which contains c copies of the $\mathrm{BY}(p + q, k)$ network.
2) Replace each $\mathrm{BY}(p + q, k)$ network with a legal TDTS topology that has the same switching capability. As a result, the overall topology of the $\mathrm{Log}_2(N, k, c)$ is also a legal TDTS topology.
3) Time compress the overall topology into a TDM switch.

There are many TDTS topologies that can be used in Step 2). We present several of them in this paper and show that they lead to different maximum delays in the network.

B. Topology Transformation

Channel Graphs: The channel graph between an input x and an output y is the union of all paths connecting x and y. In a channel graph [Fig. 6(b)], the vertices represent the links in the original topology [4] and edges represent the internal paths through a switch node for their vertices [Fig. 5(b)]. The channel graphs in our discussion are simple graphs, meaning no multiple edges exist between two vertices. Two channel graphs X and Y are called isomorphic if there is a bijection between vertices of X and Y

$$t : V(X) \rightarrow V(Y)$$

such that if and only if any two vertices u and ν from X are adjacent, then $t(u)$ and $t(\nu)$ are adjacent in Y. Simply put, two isomorphic graphs have identical properties.

New Topology: We now describe the key step in the proposed method. Since in each copy the extra k stages are

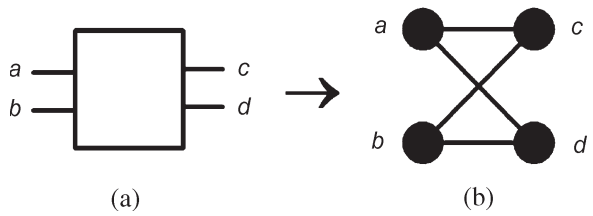

Fig. 5. (a) Original switch topology. (b) Channel graph model where a vertex represents an input and an output link in the original topology, and an edge represents an internal path through a node.

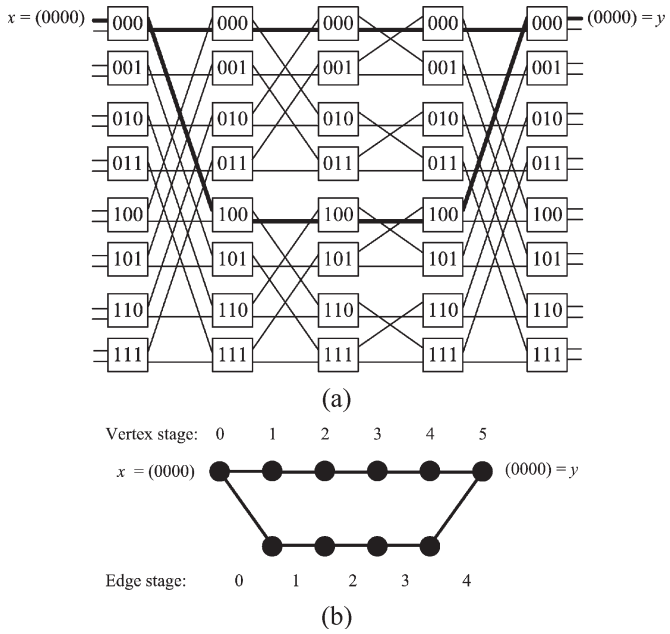

Fig. 6. (a) Paths between input (0000) and output (0000) in two different networks. (b) Channel graph.

always the mirror image of the first k stages, our discussion on topology transformation will focus on the networks without extra stages. The BY$(p+q,k)$ network has $(p+q+k-1)$ link stages, and they are numbered from 0 to $(p+q+k-2)$ (Fig. 3). Besides the two-tuple (t,s) notation used in Property 1, we also use a binary number $(x_{p+q-1},\ldots,x_1x_0)_l$ to represent a link position on the left and $(x_{p+q-1},\ldots,x_1x_0)_r$ on the right, where x_0 is the least significant bit. Let $X_{p+q} = (x_{p+q-1}x_{p+q-2},\ldots,x_1x_0)$. The original connection pattern in the ith link stage of the BY network can be described as

$$(X_{p+q})_l \mapsto (F_i(X_{p+q}))_r, \quad 0 \le i \le p+q-2 \qquad (2)$$

where F_i is

$$F_i(X_{p+q}) = \begin{cases} (x_{p+q-1},\ldots,\overline{x}_{p+q-1-i},\ldots,x_0), & \text{if } x_0 = 0 \\ (x_{p+q-1},\ldots,x_{p+q-1-i},\ldots,x_0), & \text{if } x_0 = 1. \end{cases} \qquad (3)$$

We now replace BY$(p+q,k)$ with a legal TDTS topology that has an isomorphic channel graph. The replacement network has the same number of stages. The topology of the replacement network is given in the following formula:

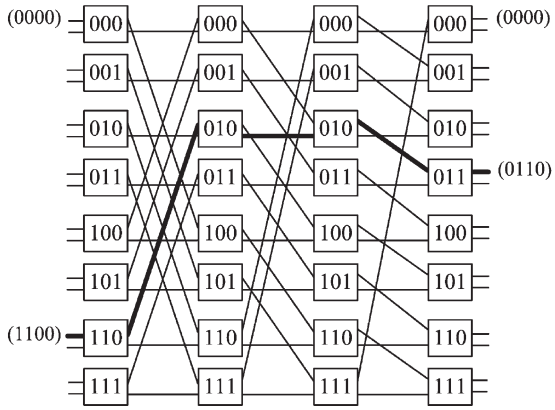

Fig. 7. TC_1 (4, 0) with each switch labeled.

$$(X_{p+q})_l \mapsto (G_i(X_{p+q}))_r, \quad 0 \le i \le p+q-2 \qquad (4)$$

where $G_i(X_{p+q})$ is

$$G_i(X_{p+q}) = \begin{cases} \left((x_{p+q-1},\ldots,x_0)+2^{p+q-1-i}\right) \bmod nd, & \text{if } x_0 = 0 \\ (x_{p+q-1},\ldots,x_0), & \text{if } x_0 = 1. \end{cases} \qquad (5)$$

In the new topology, we can see that the first output link of each node in stage i, $0 \le i \le p+q-2$, is shifted downward (in a modular sense) by $2^{p+q-i-1}$. We are going to show that the topology defined by (4) is a legal TDTS topology. We use TC_1 (time compressible, type 1) to name the new network defined by (4). $TC_1(p+q,0)$ represents a $(p+q)$-stage TC_1 network without extra stages, and $TC_1(p+q,k)$ is a network created by adding k stages (which are mirror image of the first k stages) to the $TC_1(p+q,0)$ network.

Property 3: There is a unique path from an input to an output in a $TC_1(p+q,0)$ network.

Proof: Given an input $u = (u_{p+q-1},\ldots,u_1,u_0)$ and an output $\nu = (\nu_{p+q-1},\ldots,\nu_1,\nu_0)$, the node numbers on which the two are located are $(u_{p+q-1},\ldots,u_1)$ and $(\nu_{p+q-1},\ldots,\nu_1)$, respectively. Let $(k_{p+q-1},\ldots,k_1) = ((\nu_{p+q-1},\ldots,\nu_1) - (u_{p+q-1},\ldots,u_1)) \bmod (nd/2)$. Then, the path from u to ν is determined by the path vector $(k_{p+q-1},\ldots,k_1,\nu_0)$, where ν_0 is the last bit of ν. We trace the route starting from the node where u is located (node stage 0). The node has two output links. If k_{p+q-1} is 0, use the *lower* link; 1, *upper* link. In general, a node in stage i will use bit k_{p+q-i} to determine which of the two output links for the path in a similar way. The last bit ν_0 of the path vector will determine the output link of the node in the last stage. Since different ν and u will lead to different path vector $(k_{p+q-1},\ldots,k_1,\nu_0)$, the path is unique for any input/output pair. ■

Fig. 7 shows the path from input 1100 to output 0110. The path vector is $(k_3,k_2,k_1,\nu_0) = (1010)$, and its path is indicated by the heavy lines.

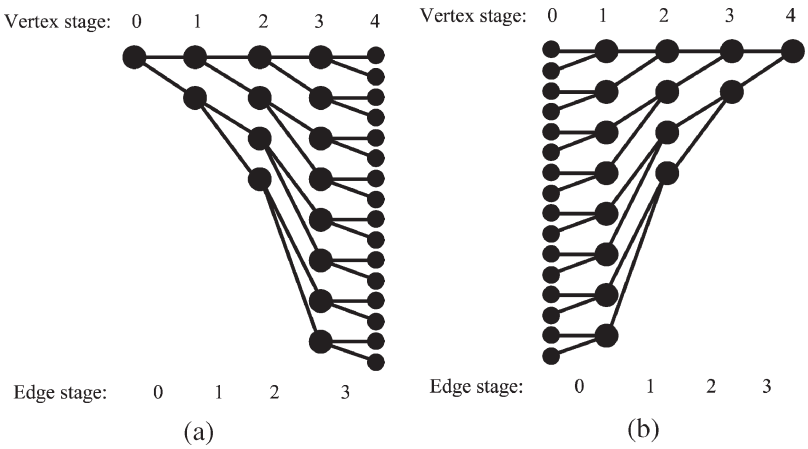

Fig. 8. (a) Paths from one input to all outputs form a full binary tree. (b) Paths from all inputs to one output also form a full binary tree.

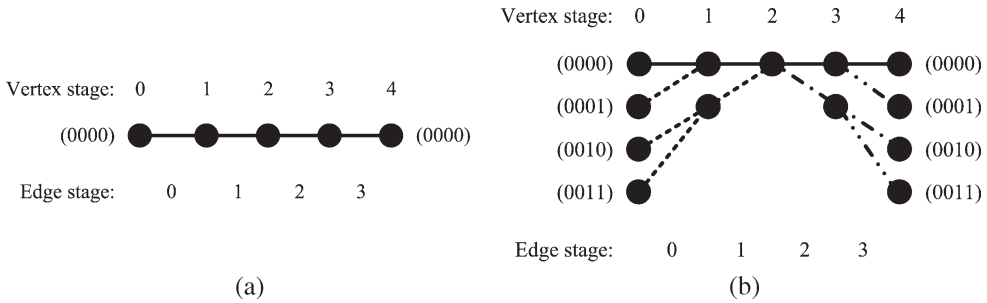

Fig. 9. (a) Channel graph from an input to an output. (b) Number of intersecting paths at each vertex in the channel graph between input 0000 and output 0000.

Property 4: In the $\mathrm{TC}_1(p+q,0)$ network, the channel graph from an input to all outputs forms a full binary tree (no leaf missing). The channel graph from all inputs to one output also forms a full binary tree.

Proof: An input can reach all outputs because there is a unique path from an input to an output (Property 3). Consider the channel graph from one input to all outputs. Since the number of vertices reachable from an inlet vertex only increases by a factor of 2, unless the channel graph is a full tree, an input cannot reach all outputs. Similarly, we can conclude that the channel graph form all inputs to one output is also a full binary tree [in the reverse direction, see Fig. 8(b)]. ■

One result derived from Property 4 is that the number of intersection paths at a vertex of stage i will be $\min\{2^i, 2^{p+q-i}\}$ (Fig. 9) in the $\mathrm{TC}_1(p+q,0)$ network. This is the same as that in a BY network.

Property 5: The channel graph of a $\mathrm{TC}_1(p+q,k)$ network is isomorphic to that of a $\mathrm{BY}(p+q,k)$ network.

Proof: When $k=0$, the channel graph from an input to an output consists of only one path (Property 3). Obviously, it is isomorphic to that of a $\mathrm{BY}(p+q,0)$ network. In addition, the channel graph from an input to all outputs is a full binary tree (Property 4) that consists of two subtrees rooted at vertices a and b (Fig. 10). Let y be an output vertex. By the topological rule given by (5), if $y \in a$-subtree, then $((y+2^{p+q-1}-1) \bmod 2^{p+q}) \in b$-subtree.

When $k=1$, consider the channel graph from input u to output y in Fig. 10. By adding one extra stage, the destination y can reach two outputs a' and b' vertices in the $\mathrm{TC}_1(p+q,0)$ network. Because the last stage is just the mirror image of the first stage, a' and b' must be separated by $(2^{p+q-1}-1)$. From the discussion on $k=0$, if a' and b' are separated by $(2^{p+q-1}-1)$, they cannot belong to the same subtree. That is, if $a' \in a$-subtree (or b-subtree), then $b' \in b$-subtree (or a-subtree). Also, there is a unique path from input u to a' and b' (Property 3). Therefore, the channel graph of $\mathrm{TC}_1(p+q,1)$ will be the same as that in Fig. 6(b). This means that it is isomorphic to that of $\mathrm{BY}(p+q,1)$.

When $k>1$, we can prove in a similar way that the channel graph from one input to an output is isomorphic to that of a $\mathrm{BY}(p+q,k)$ network. ■

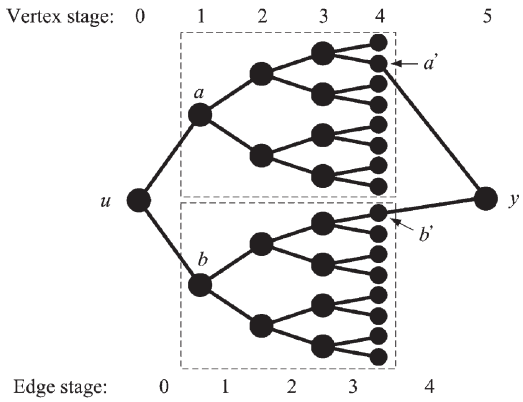

Fig. 10. Adding one extra stage allows two vertices a' and b' in the $\mathrm{TC}_1(p+q,0)$ to reach the real destination. One of the two vertices a' and b' must be in two different subtrees (rooted at a and b).

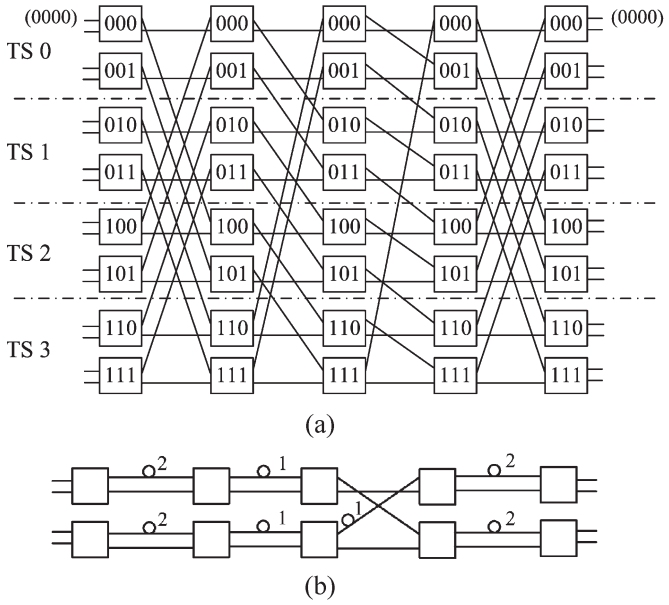

Fig. 11. (a) TC_1 (4, 1) topology is a legal TDTS topology with frame size $= 4$ and input size $= 4$. (b) TDM switch derived from time compressing the topology of Fig. 11.

Property 6: The $TC_1(p+q,k)$ topology given by (4) is a legal TDTS topology with frame size d and input size n, where $n = 2^p$ and $d = 2^q$.

Proof: We first consider the $TC_1(p+q,0)$ network topology. Each link position can also be represented as a binary number $X_{p+q}(= (x_{p+q-1}, \ldots, x_1, x_0))$ or by a two-tuple (t,s), where $0 \le t \le (d-1)$ and $0 \le s \le (n-1)$, as used in Property 1. We use both in proving this property.

Given $(x_{p+q-1}, \ldots, x_1, x_0)_l$ in any stage, when $x_0 = 1$, it is connected to the same position on the right, i.e., $(x_{p+q-1}, \ldots, x_1, x_0)_l \mapsto (x_{p+q-1}, \ldots, x_1, x_0)_r$ (Fig. 7). Property 1 obviously holds. We only need to check the mapping for $(x_{p+q-1}, \ldots, x_1, x_0)_l$ with $x_0 = 0$. According to (4), the interconnection pattern is $(X_{p+q})_l \mapsto (G_i(X_{p+q}))_r$. Let $(X_{p+q})_l = (t,j)_l$ and $(G_i(X_{p+q}))_r = (u,\nu)_r$. The difference between $(X_{p+q})_l$ and $(G_i(X_{p+q}))_r$ is

$$(G_i(X_{p+q}))_r - (X_{p+q})_l) \bmod nd = 2^{p+q-1-i}. \qquad (6)$$

In the TDTS topology, there are $n(= 2^p)$ links per time-slot. Thus, the time-slot difference between a link position $(X_{p+q})_l$ and its mapping $(G_i(X_{p+q}))_r$ is (2^{q-1-i}). Thus, given $(t,j)_l \mapsto (u,\nu)_r$, we have $u = ((t + 2^{q-1-i}) \bmod d)$. Now, let us compute the mapping for $((t+e) \bmod d, j)_l$.

$$\begin{aligned}((t+e)\bmod d, j)_l &\mapsto (G_i\left((t+e)\bmod d\right), j)_r \\ &= \left(\left((t+e) + 2^{q-1-i}\right) \bmod d, \nu\ \right)_r \\ &= \left((u+e)\bmod d, \nu\right)_r . \qquad (7)\end{aligned}$$

Thus, Property 1 is satisfied. For the $TC_1(p+q,k)$ network, the extra k stages are the mirror image of the first k stages. By Property 2, $TC_1(p+q,k)$ is also a legal TDTS topology (see Fig. 11). ■

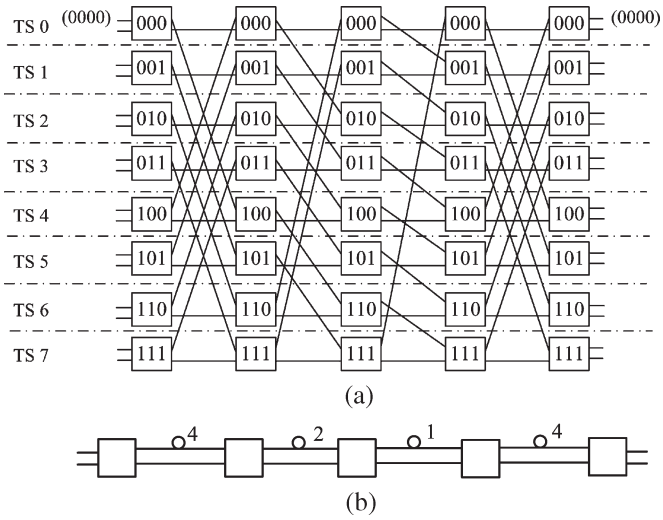

Fig. 12. (a) Same $TC_1(4, 1)$ topology in Fig. 11 can also be considered as a legal TDTS topology with frame size $= 8$ and input size $= 2$. (b) Time-compressed TDM switch.

Because the topology shown in Fig. 11 is a legal TDTS topology (Property 5), we can time compress it into a delay-unit-based TDM switch, and it is shown in Fig. 12. Another important property of TC_1 is that it depends only on $(p+q)$ and it is valid for all different (p,q) combinations. For example, the same topology in Fig. 11 can also be considered as a TDTS topology of $n = 2$, $d = 8$ [Fig. 12(a)]. Its time-compressed TDM switch is shown in Fig. 12(b). This flexibility comes at the expense of a larger maximum delay in the network, as will be discussed in Section III-C.

Final Architecture: The construction of the nonblocking $\mathrm{Log}_2(N,k,c)$ network is based on its channel graph [12] and the number of intersecting paths at each vertex of the channel graph. From Properties 3–6, we find that the channel graph of the $TC_1(p+q,k)$ network is isomorphic to that of the $BY(p+q,k)$ network, and the number of intersection paths at each vertex in the channel graph is also the same. Thus, if we replace the $BY(p+q,k)$ network in the $\mathrm{Log}_2(N,k,c)$ network with a $TC_1(p+q,k)$ network, the number of copies remains unchanged. The overall topology will be a legal TDTS topology.

Our original design is for $n = 4$, $d = 4$. We use the topology in Fig. 11 to replace the BY network. The overall topology is given in Fig. 13. Note that the first and the last stage in Fig. 13 are multiplexers, and they can be implemented with 2×2 couplers as well.

C. Other TDTS Topologies

There are many other TDTS topologies that can be used to replace the BY networks. We show two below. The first one is the topology given by

$$\begin{aligned}&(X_{p+q})_l \mapsto (G_i(X_{p+q}))_r , \quad 0 \le i \le q-1 \\ &(X_{p+q})_l \mapsto (F_i(X_{p+q}))_r , \quad q \le i \le p+q-2 \qquad (8)\end{aligned}$$

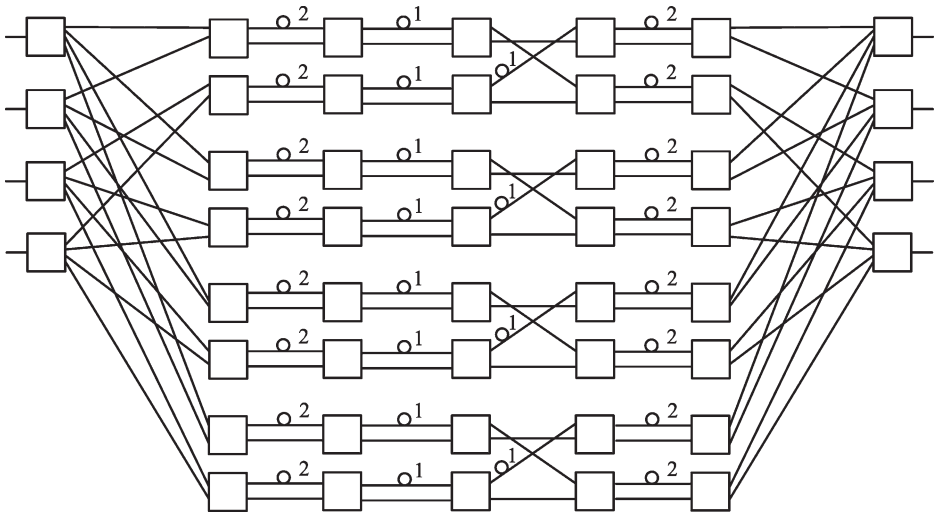

Fig. 13. Time-compressed SNB TDM switch with four inputs and frame size $= 4$.

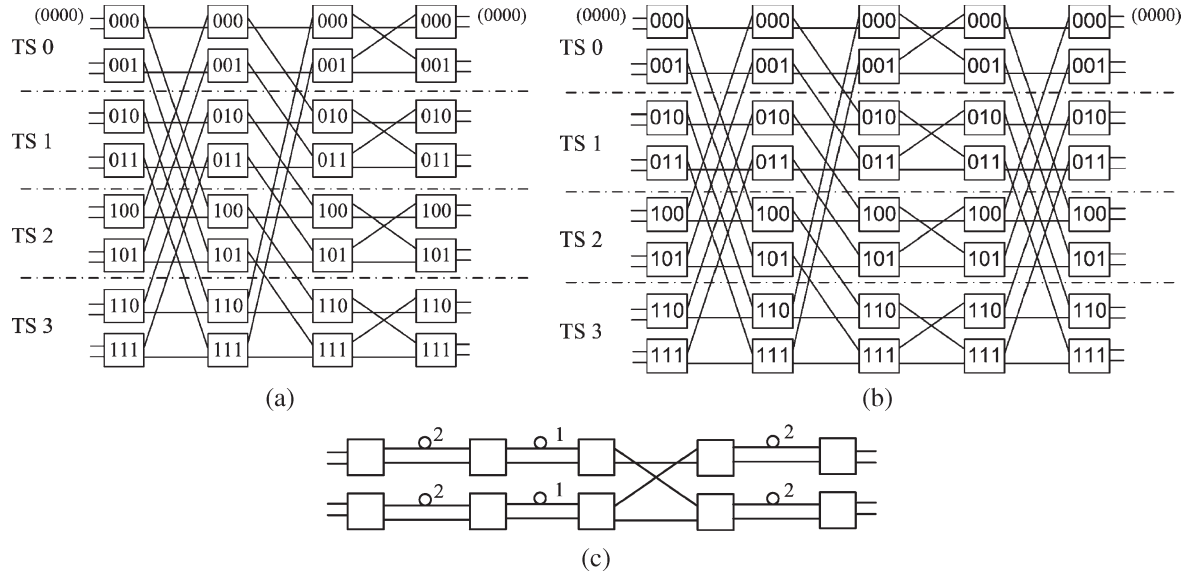

Fig. 14. (a) $TC_2(4, 0)$ network. (b) $TC_2(4, 1)$ network (add one extra stage). (c) It can be time compressed into a TDM switch with four inputs and four slots (frame size).

where F and G are given in (3) and (5). Following the same arguments we use for Properties 3–5, it is not difficult to show that TC_2 has isomorphic channel graphs as that of BY and TC_1. Therefore, it can also be used to replace the BY network in Fig. 13 without changing the number of copies required.

The third type of legal TDTS topology is given in Fig. 15 which is the reversed topology of that in Fig. 14. The topology is described by

$$\begin{aligned}(X_{p+q})_l &\mapsto (H_i(X_{p+q}))_r, \quad 0 \le i \le p-2\\ (X_{p+q})_l &\mapsto (I_i(X_{p+q}))_r, \quad p-1 \le i \le p+q-2\end{aligned} \tag{9}$$

where

$$H_i(X_{p+q}) = \begin{cases} (x_{p+q-1}, \ldots, \overline{x}_{i+1}, \ldots, x_0), & \text{if } x_0 = 0\\ (x_{p+q-1}, \ldots, x_{i+1}, \ldots, x_0), & \text{if } x_0 = 1.\end{cases} \tag{10}$$

and

$$I_i(X_{p+q}) = \begin{cases} \left((x_{p+q-1}, \ldots, x_0) + 2^{i+1}\right) \bmod nd, & \text{if } x_0 = 0\\ (x_{p+q-1}, \ldots, x_0), & \text{if } x_0 = 1.\end{cases} \tag{11}$$

Following similar arguments used for TC_1 networks, we can also show that it is a legal TDTS topology. Its time-compressed TDM switch is shown in Fig. 15(c). All three require the same number of couplers, and their space switching complexities are the same. But, the difference lies in the delay. Among the three, the TDM switch in Fig. 15 has the minimum value of the maximum delay. As a matter of fact, it is only about half the value of that in TDM switch given Fig. 12.

Compared with the rearrangeable networks in [6], the SNB networks discussed in this paper obviously have more couplers. But, the crosstalk is lower as they contain fewer stages. Table I shows some examples (The multiplexing and demultiplexing stages are not counted as they do not generate crosstalk).

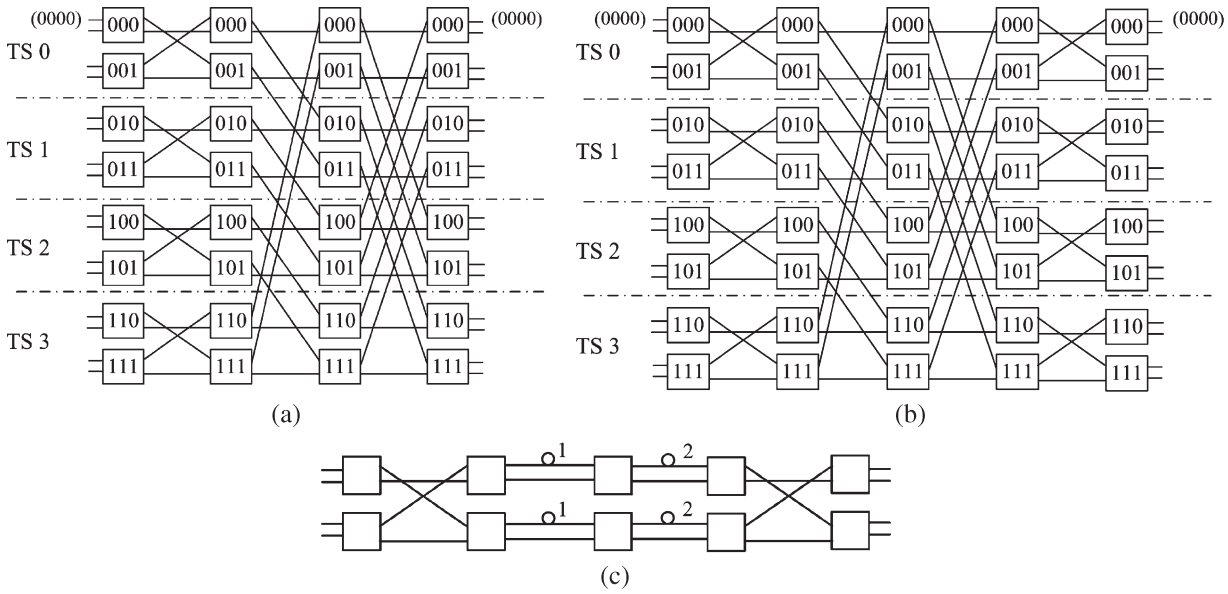

Fig. 15. (a) $TC_3(4, 0)$ network. (b) $TC_3(4, 1)$ network. (c) $TC_3(4, 1)$ can be time compressed into a TDM switch (inputs and four slots/per frame).

TABLE I
NUMBER OF CROSSPOINTS AND THE NUMBER OF STAGES IN REARRANGEABLE NETWORKS [6] AND SNB NETWORKS DISCUSSED IN THIS PAPER (SNB: STRICTLY NONBLOCKING, RNB: REARRANGEABLE NONBLOCKING)

TDM	Size/# of input or output/# of time slot per frame	Type	Number of Stages	Switch Count
TC_1, TC_2, TC_3.	$N = 8, n = 2, d = 4$	SNB	4	12
	$N = 16, n = 4, d = 4$		5	40
TDM with no frame integrity in [6].	$N = 8, n = 2, d = 4$	RNB	5	5
	$N = 16, n = 4, d = 4$		7	13

IV. CONCLUSION

In this paper, we have presented the design principles and techniques for building nonblocking optical TDM switches that do not use TSIs. Since optical TSIs are difficult to build and have many drawbacks, like severe signal attenuation in the system, a TSI-free architecture will be attractive for photonic switching technologies. In contrast to previous works, we focus on SNB network in this paper. We show several topologies that can be used for our purpose, and each leads to a different value in the maximum delay of the network. The design principles can also be applied to space/wavelength photonic switching systems, as the one discussed in [8].

REFERENCES

[1] D. Bishop *et al.*, "The rise of optical switching," *Sci. Amer.*, vol. 284, no. 1, pp. 88–94, Jan. 2001.
[2] C.-T. Lea, "Expanding the switching capability of optical cross-connects," *IEEE Trans. Commun.*, vol. 53, no. 11, pp. 1940–1944, Nov. 2005.
[3] K. Padmanabhan and A. Netravali, "Dilated networks for photonic switching," *IEEE Trans. Commun.*, vol. COM-35, no. 12, pp. 1357–1365, Dec. 1987.
[4] C.-T. Lea, "Bipartite graph design principle for photonic switching systems," *IEEE Trans. Commun.*, vol. COM-38, no. 4, pp. 529–538, Apr. 1990.
[5] M. J. Marcus, "Space-time equivalents in connecting networks," in *Proc. ICC*, 1970, pp. 35.25–35.31.
[6] D. K. Hunter and D. G. Smith, "New architectures for optical TDM switching," *J. Lightw. Technol.*, vol. 11, no. 3, pp. 495–511, Mar. 1993.
[7] R. Thompson and D. K. Hunter, "Elementary photonic switching modules in three divisions," *IEEE J. Sel. Areas Commun.*, vol. 14, no. 2, pp. 362–373, Feb. 1996.
[8] N. Antoniades, S. J. B. Yoo, K. Bala, G. Ellinas, and T. Stern, "An architecture for a wavelength-interchanging cross-connect utilizing parametric wavelength converters," *J. Lightw. Technol.*, vol. 17, no. 7, pp. 1113–1125, Jul. 1999.
[9] V. E. Benes, *Mathematical Theory of Connecting Networks and Telephone Traffic*. New York: Academic, 1965.
[10] F. K. Hwang, *The Mathematical Theory of Nonblocking Switching Networks*. Singapore: World Scientific, Feb. 1999.
[11] F. H. Chang, J. Y. Guo, and F. K. Hwang, "Wide-sense nonblocking for multi-$\log_d N$ networks under various routing strategies," *Theor. Comput. Sci.*, vol. 352, no. 1–3, pp. 232–239, 2006.
[12] D. J. Shyy and C. T. Lea, "$\log_2(N, m, p)$ strictly nonblocking networks," *IEEE Trans. Commun.*, vol. 39, no. 10, pp. 1502–1510, Oct. 1991.
[13] R. A. Thompson and P. P. Giordano, "An experimental photonic time slot interchanger using optical fibers as reentrant delay-line memory," *J. Lightw. Technol.*, vol. LT-5, no. 1, pp. 154–162, Jan. 1987.
[14] A. Chen, A. Wong, and C.-T. Lea, "Routing and time-slot assignment in optical TDM networks," *IEEE J. Sel. Areas Commun.*, vol. 22, no. 9, pp. 1648–1657, Nov. 2004.
[15] C.-T. Lea, "Multi-$\log_2 N$ networks and their applications in high-speed electronic and photonic switching systems," *IEEE Trans. Commun.*, vol. COM-38, no. 10, pp. 1740–1749, Oct. 1990.
[16] D. K. Hunter and D. G. Smith, "Optical TDM switching architectures with reduced control complexity," *Proc. Inst. Elect. Eng.—I*, vol. 140, no. 3, pp. 220–228, Jun. 1993.

Chin-Tau Lea (S'81–M'82–SM'93) received the B.S. and M.S. degrees from National Taiwan University, Tainan, Taiwan, R.O.C., in 1976 and 1978, respectively, and the Ph.D. degree from the University of Washington, Seattle, in 1982, all in electrical engineering.

From 1982 to 1985, he was with AT&T Bell Laboratories, and from 1985 to 1995, he was with Georgia Institute of Technology, Atlanta. Since 1996, he has been with Hong Kong University of Science and Technology (HKUST), where he is currently a Professor. His research interests are in the areas of switching and networking. He also holds six U.S. patents.

Dr. Lea is currently on the Editorial Board of IEEE JOURNAL OF SELECTED AREAS IN COMMUNICATIONS and of *Computer Networks.* He received the IEEE Jack Neubauer Paper Award in 1998 and the School of Engineering Teaching Award from HKUST in 1998.

Bey-Chi Lin received the B.S. degree in mathematics education from National Taichung Teachers College, Taiwan, R.O.C., in 1999 and the Ph.D. degree in applied mathematics from National Chiao Tung University, Hsinchu, Taiwan, in 2005.

She is currently a Research Assistant with Hong Kong University of Science and Technology. Her research interests include switching network analysis and combinatorial mathematics.

Hamdi Mounir received the B.S. degree from University of Louisiana, Shreveport, in 1985, and the M.S. and Ph.D. degrees from University of Pittsburgh, Pittsburgh, PA, in 1987 and 1991, respectively, all in electrical engineering.

Since 1991, he has been a Faculty Member with the Department of Computer Science, Hong Kong University of Science and Technology (HKUST), where he is currently a Full Professor of computer science and engineering.

Dr. Mounir is/was on the Editorial Board of IEEE TRANSACTIONS ON COMMUNICATIONS, *IEEE Communication Magazine, Computer Networks, Wireless Communications and Mobile Computing,* and *Parallel Computing.* He has chaired more than seven international conferences. He is/was the Chair of IEEE Communications Society Technical Committee on Transmissions, Access and Optical Systems, and Vice-Chair of the Optical Networking Technical Committee, as well as a member of the ComSoc technical activities council. He also received the Best Ten Lecturers Award and the Distinguished Engineering Teaching Appreciation Award from HKUST.